



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,955	08/31/2001	Arulkumar P. Shanmugasundram	5918/04/FPS/MMCS/APC/DV	2623
32588	7590	07/26/2005	EXAMINER	UMEZ ERONINI, LYNETTE T

APPLIED MATERIALS, INC.
2881 SCOTT BLVD. M/S 2061
SANTA CLARA, CA 95050

ART UNIT PAPER NUMBER

1765

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/943,955	SHANMUGASUNDRAM ET AL.
	Examiner	Art Unit
	Lynette T. Umez-Eronini	1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 13 June 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-27 and 34 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-27 and 34 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 31 August 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 5/18/2005.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

This communication is in response to Applicants' Remarks in Amendment filed 6/13/2005, which were persuasive in showing the finality of the last Office Action was improper because it rejected unamended claims over newly cited art. Hence, a new Office Action is presented.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 3-5, 14, 15, 16, 17; 2; and 21-24 and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell et al. (US 6,230,069 B1) in view of Adams et al. (US 5,664,990).

Campbell teaches a method of for controlling post-polish thickness of wafer layers by chemical mechanical polishing tools (column 3, lines 39-44). The method measures pre-polish thickness and post-polish thickness of wafer layers (column 3, lines 64-67 and column 4, lines 9-35) and uses the thickness measurements to control a polishing time input to the polish tool **220** for a subsequent wafer run (column 4, lines 10-14 and column 4, lines 47-67). The aforementioned read on,

A method of producing a target wafer thickness profile in a polishing operation, comprising:

- a) providing a model for a wafer polishing and identifies a wafer material removal rate in a polishing step, wherein the model is based on measurements of one or more wafers that have completed the polishing step; and
- (b) polishing a wafer using a polishing recipe based on the model that generates a target thickness profile for each region, **in claims 1, 3-5, and 14-17.**

A method of controlling surface non-uniformity of a wafer in a polishing operation, comprising:

- a) providing a model for a wafer polishing and identifies a wafer material removal rate in a polishing step, wherein the model is based on measurements of one or more wafers that have completed the polishing step
- b) polishing a wafer using a first polishing recipe;

c) determining a wafer thickness profile for the post-polished wafer of step (b);

and

d) calculating an updated polishing model based upon the wafer thickness profile of step (c) and the model of step (a) and updating the first polishing recipe based on the updated model to maintain a target wafer thickness profile, **in claim 2**; and

A method of determining a model for wafer thickness profile, comprising:

(a) measuring pre-polished wafer thickness in a region defined on one or more wafers;

(b) polishing the one or more wafers, wherein polishing comprises polishing the one or more wafers in a plurality of polishing steps;

(c) measuring the wafer material removal rate for the one or more wafers after each of the polishing steps of step (b);

(d) providing a model defining the effect of tool state on polishing effectiveness;

and

(e) recording the pre-polished and post-polished wafer thicknesses on a recordable medium, **in claims 21-24**; and

A method of producing a target wafer thickness profile in a polishing operation, comprising:

a) providing a model for a wafer polishing that identifies a region on a wafer, identifies a wafer material removal rate in a polishing step, and defines the effect of the tool state on polishing effectiveness; and

(b) polishing a wafer using a polishing recipe based on the model that generates a target thickness profile for each region, **in claim 34.**

Campbell differs in failing to teach a plurality of substantially annular regions on a wafer, **in claims 1, 2, 21, and 34.**

Adams teaches a wafer is rotated against a polishing pad in a typical CMP apparatus (column 1, line s 20-21) and discloses there is inevitable an annular region about the periphery of a wafer where the polishing is not uniform (column 5, lines 28-30), which suggests a wafer may have a plurality of substantially annular regions.

Since Adams illustrates annular regions on a wafer, then it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to polish wafers having annular regions for the purpose of effecting the polishing method of the claimed invention.

3. Claims 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell (US '069 B1) in view of Adams (US '990), as applied to claim 1 above.

Campbell in view of Adams differs in failing to specify the number and type of polishing stations used in the polishing step.

It would have been obvious to one having ordinary skill in the art of the time of the claimed invention to employ known methods of polishing a wafer in a polishing station as well as in a plurality of polishing stations as claimed by applicants for the purpose of speeding up the step of polishing semiconductor wafers.

Allowable Subject Matter

4. Claims 18-20, and 25-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
5. The following is a statement of reasons for the indication of allowable subject matter:

As to claims 18-20, the prior art of record taken alone or in combination fails to suggest, teach, or render obvious a method of producing a target wafer thickness profile in a polishing operation, wherein the wafer removal for a region j ($AR'{}_j$) in the model of step (a) is determined according to the equation as recited in claim 18, and in combination with the rest of the limitations of the said claims.

As to claims 25-27, the prior art of record taken alone or in combination fails to suggest, teach, or render obvious a method of determining a model for wafer thickness profile comprising: wherein the wafer removal for a region j ($AR'{}_j$) in the model of step (a) is determined according to the equation as recited in claim 25 and in combination with the rest of the limitations of the said claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1-27 and 34 have been considered but are moot in view of the new ground(s) of rejection because "a method of providing a target thickness profile in a polishing operation, comprising . . . --wherein the model is based on measurement of one or more wafer that have completed the polishing step-- .

..." as recited in (currently amended) Claim 1 was not taught by the former prior art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

Itue

June 24, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER
